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Application Serial No.: 10/658700
For the Office Action Dated: December 29, 2006

REMARKS

This Amendment is in response to the Office Action mailed on December 29, 2006. Claims 1, 6 and 7 are amended editorially and are supported, for example, in the specification on page 11, line 31-page 12, line 6 and Figure 4. Claim 4 is cancelled without prejudice or disclaimer. No new matter is added. Claims 1-3 and 5-9 are pending.

103(a) Rejections:

Claims 1-4 and 8 are rejected as being unpatentable over Koizumi (US Patent No. 7,129,985) in view of Yonemoto (US Patent No. 6,483,541) and further in view of Mutoh (A 1v Multi-Threshold Voltage CMOS DSP with an Efficient Power Management Technique for Mobile Phone Application). This rejection is traversed.

Claim 1 is directed to an imaging device chip set that requires, among other features, an imaging device chip set that has an imaging chip and a DSP chip. The DSP chip includes a timing generating circuit and a digital signal processing circuit that are both formed with CMOS transistors. The imaging chip includes a horizontal scanning circuit, a vertical scanning circuit and a plurality of unit pixels that are all formed with transistors of a same conductivity type. Also, at least a part of the horizontal scanning circuit and the vertical scanning circuit are formed with dynamic shift register circuits composed of transistors of the same conductivity type and capacitors. An advantage of having the horizontal and vertical scanning circuits formed with dynamic shift register circuits formed of the transistors of the same conductivity type and capacitors is that a flow-through current due to switching of CMOS circuits can be avoided. By avoiding flow-through current, the present invention achieves an imaging device chip set that reduces noise, avoids an error in the selection of pixels and prevents stoppage of the shift register.

The combination of Koizumi, Yonemoto and Mutoh does not teach or suggest these features. The rejection relies on Yonemoto for suggesting the incorporation of multiple pixel units of the same conductivity type. Yonemoto is directed to a solid state imaging device that has a large number of pixel transistors (11), shown as NMOS transistors in Figure 1, and a vertical scanning circuit (15) and a horizontal scanning

circuit (16) (see column 10, lines 12-33). However, nowhere does Yonemoto teach or suggest horizontal and vertical scanning circuits formed with transistors of a same conductivity type or that the horizontal and vertical scanning circuits are formed with dynamic shift registers as required by claim 1. Accordingly, Yonemoto also does not teach or suggest dynamic shift registers composed of transistors of the same conductivity type and capacitors. Neither Koizumi nor Mutoh overcome these deficiencies of Yonemoto. For at least these reasons, claim 1 is not unpatentable by the combination of Koizumi, Yonemoto and Mutoh and should be allowed. Claims 2-4 and 8 depend from claim 1 and should be allowed for at least the same reasons.

Claim 5 is rejected as being unpatentable over Koizumi in view of Yonemoto further in view of Mutoh and also in view of Ewedemi (US Patent No. 6,985,181). This rejection is traversed. Claim 5 depends from claim 1 and should be allowed for at least the same reasons described above. Applicants do not concede the correctness of this rejection.

Claims 6 and 7 are rejected as being unpatentable over Koizumi in view of Yonemoto further in view of Mutoh also in view of Ewedemi and lastly in view of Suda (US Patent No. 6,441,441). This rejection is traversed. Claims 6 and 7 depend from claim 1 and should be allowed for at least the same reasons described above. Applicants do not concede the correctness of this rejection.

Claim 9 is rejected as being unpatentable over Koizumi in view of Yonemoto further in view of Mutoh and also in view of Miyamoto (US Patent No. 6, 518,999). This rejection is traversed. Claim 9 depends from claim 1 and should be allowed for at least the same reasons described above. Applicants do not concede the correctness of this rejection.

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Conclusion:

Applicants respectfully assert claims 1-3 and 5-9 are now in condition for allowance. If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Applicants' primary attorney-of record, Douglas P. Mueller (Reg. No. 30,300), at (612) 455-3804.

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Dated: March 29, 2007

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